**ESET 219 Digital Electronics**

Laboratory Report

Lab 6

Flip Flop Circuits

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All of the information contained in this report is my own work that I completed as part of this lab assignment. I have not used results or content from any unauthorized sources or fellow students.

Ogochukwu Ezuma Date: 11/17/2023

**Introduction**

The objective of task 1 for this lab was to display the timing diagram of a D flip flop circuit. Task 2 required the creation of a circuit of a countdown device, its outputs being shown through a 7-segment display. It’s state table was given. the overall purpose of the lab was to examine flip flop behavior and use flip flops in circuit design. The focus on the lab is the D flip flop.

**Background**

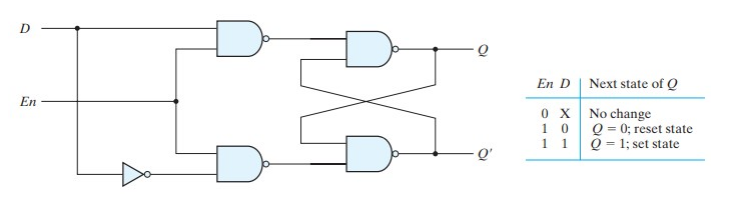
A D flip flop works as a memory element, which takes one input and returns an output in relation the previous state of the device. It accomplishes this feat through feedback, the configuration of looping its output back to its input, storing said output as a state in memory. To make sense of a D flip flop, a D latch will be explained first. A D latch utilizes an input D, an enable, and feedback to put an output into a set or reset state. A door can be locked (set) or unlocked (reset) with a key. When a key is inserted and turned to locked, it is said to be latched. The key doesn’t need to remain in the lock for the door to be locked. The same analogy applies to the door being unlocked.

Figure : 0 on the output represents a reset state, while 1 represents a set state

When the enable is active, the state can be changed. The enable can act as a clock signal, switching from HIGH to LOW a certain frequency. All latches, including D latches are level triggered devices, meaning they respond to input changes within all active clock periods.

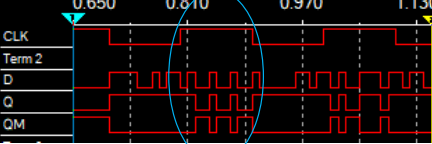


Figure : displays the timing diagram of a D latch, with input D feeding into output Q. as designated within the blue circle, multiple changes to the output can happen within each clock pulse

The characteristic of multiple changes happening within a single clock pulse may exhibit a glitch within a system. To prevent this such a behavior, it’s necessary to utilize devices that are edge triggered. Edge triggered logic components only respond to input changes at either the rising edge of a clock pulse, or the falling edge. A diagram of a diagram

Description automatically generated with medium confidence

Figure : Positive edge responses indicate an active HIGH enable/clock, while negative-edge responses represent active LOWs.

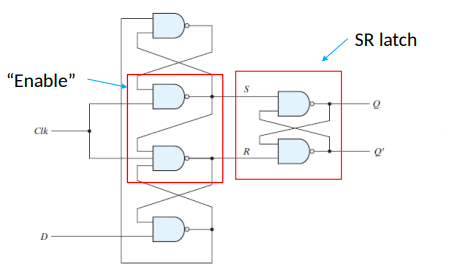
Flip Flops are logic devices that are similar in every aspect to latches, distinguished exclusively in the fact they are edge triggered. To summarize, a D flip flop is an edge triggered D latch. 

Figure : The schematic of a D flip flop. an SR latch is denoted, for D latches are derived from an SR latch.

The preset and clear inputs are inputs that affect the output disregarding the state of the clock.

State equations describe a circuit made up of memory devices as a Boolean expression. Multiple equations are needed for every circuit, to describe the outputs and to describe the states.

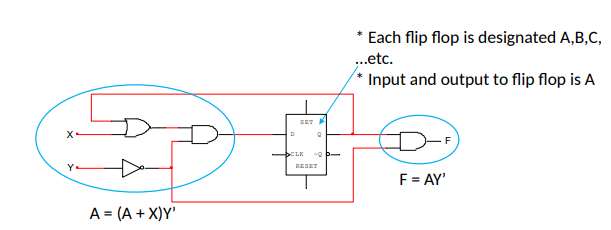


Figure : state equations listed below illustrated circuit

A state table is similar to a truth table, it describes all the possible outputs given input combinations. An example is shown in the figure below.

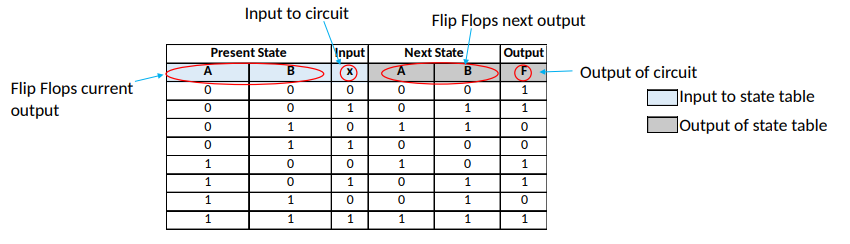


Figure : State table - Inputs include current outputs of flip flops (A,B,..etc.) and input of circuit (X,Y,..etc.). Outputs include the next outputs of flip flops (A,B,..etc.) and outputs of circuit (F,G,..etc.).

To recreate a memory circuit based off its state table, K-maps will need to be employed for each output. The state K-maps represent the input combination feeding into a D flip flop, while the output K-maps simply represent the input combination towards an output.

**Implementation**

Task 1’s objective was to model an understanding of a D flip flop truth table. So the D flip flop part (DFF) was inserted into a Quartus schematic file and attached to input pins which represented the clock input, preset (asynchronous input) input, clear (asynchronous input) input, and the D input. Its output Q was represented as an output pin. Once connections were completed and pins on the FPGA boards were assigned to their respective switches and LEDs, it resulted in the network as shown below.

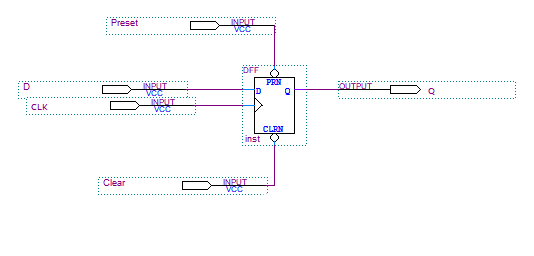


Figure : Inputs were represented as switches, while Q represented an active HIGH LED.

The following table was asked to be simulated in a timing diagram of the circuit in task 1.

|  |  |  |  |
| --- | --- | --- | --- |
| **CLK** | **Preset** | **Clear** | **D** |
| 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| ↑ | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 |
| ↑ | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 |

Table :task 1 D flip flop simulation table.

The up arrows in all instances of the clock input mean rising edge, meaning that the D input should be switched to the value it has in the row it shares with the rising clock edge, prior to the clock pulse (to ensure that clock pulse doesn’t race the D input and misread it.

To begin task 2, 4 K-maps to represent the next states (flip flops A and B) and outputs (F and G) were created in accordance to the state table provided.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Present state** | | **Input** | **Next State** | | **Outputs** | |
| A | B | x | A | B | F | G |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 |

Table : task two state table.

A grid with circles and numbers

Description automatically generated A number of feet in a row

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Figure : K map for flip flop. Figure : K map for flip flop A.

A number and a number in a row

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Figure : K Map for output F. Figure : K Map for output G.

The K maps listed above developed the resulting equations, which were then used to create the logic of the final circuit in figure 12.

***equation 1***

***equation 2***

***equation 3***

***equation 4***

A diagram of a computer

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Figure : 7 segment decoder displayed the numeric output of F and G, F being the MSB and G the LSB.

**Results**

As shown in the figure below, for task 1 all asynchronous inputs (active low) overwrite the Q output at all instances, and Q matched the input of D at the last 2 rising edges (both asynchronous inputs were inactive in both periods).

A screenshot of a computer

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Figure : timing diagram for the truth table in task 1.

The following timing diagram was presented utilizing switches and LEDs on the FPGA board to the TA.

The timing diagram below represents behavior displayed by the circuit on the 7-segment decoder. When ran on the FPGA board, every clock pulse reduced counter by 1 if X (active high) was active. If inactive, the counter will not change the output until X is active at the next rising clock edge. Once the clock reaches 0, it loops back to 3 to repeat the countdown.

A screenshot of a graph

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Figure : timing diagram for task 2

**Conclusion**

Flip flops serve as memory devices capable of storing the previous state of the device in memory as outputs. Not just for its versatile applications as shown in the countdown circuit created, but its also a key element in digital design for solving the asynchronous tendency present in latches. Being edge triggered components, they effectively nullify changes within the period of a clock pulse, and only vary the output at either the rising or falling edge of the cycle. Should asynchronous behaviour be desired, flip flops have the capacity of using separate inputs to enable such a function.